CURRICULUM & SYLLABI

M.Tech. VLSI SYSTEM DESIGN

Effective from AY: 2024-25



NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

WARANGAL, TELANGANA

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Vision and Mission of the Institute
National Institute of Technology Warangal

VISION

Towards a Global Knowledge Hub, striving continuously in pursuit of excellence in Education, Research, Entrepreneurship and Technological services to the society

MISSION

- Imparting total quality education to develop innovative, entrepreneurial and ethical future professionals fit for globally competitive environment.
- Allowing stake holders to share our reservoir of experience in education and knowledge for mutual enrichment in the field of technical education.
- Fostering product-oriented research for establishing a self-sustaining and wealth creating centre to serve the societal needs.

Vision and Mission of the Department
Electronics and Communication Engineering

VISION

Create an Educational environment to prepare the students to meet the challenges of modern electronics and communication Industry through state of art technical knowledge and innovative approaches.

MISSION

- To create learning, Development and testing environment to meet ever challenging needs of the Electronic Industry.
- To create entrepreneurial environment and industry interaction for mutual benefit.
- To be a global partner in training human resources in the field of chip design, instrumentation and networking.
- To associate with international reputed institution for academic excellence and collaborative research.

Program: M.Tech. VLSI System Design

Program Educational Objectives

PEO-1	Design of digital, analog and mixed signal integrated circuits using appropriate EDA tools, computational techniques, algorithms and develop testing methods.
PEO-2	Model passive and active devices suiting advances in IC fabrication technology.
PEO-3	Develop VLSI architectures optimized for constrained environments, RF systems and protocols.
PEO-4	Communicate effectively and convey ideas using innovative engineering tools.
PEO-5	Pursue lifelong learning as a means of enhancing knowledge base and skills necessary to contribute to the improvement of their profession and community.

Program Articulation Matrix

PEO / Mission Statements	PEO-1	PEO-2	PEO-3	PEO-4	PEO-5
To create learning, development and testing environment to meet ever challenging needs of the Electronic industry.	3	3	3	2	2
To create entrepreneurial environment and industry interaction for mutual benefit.	2	2	2	3	3
To be a global partner in Training the human resource in the fields of Chip Design, Instrumentation and Networking.	2	3	2	2	3
To associate with internationally reputed Institutions for academic excellence and collaborative research.	2	2	2	2	3

1 - Slightly; 2 - Moderately; 3 - Substantially

Program: M.Tech. VLSI System Design

Program Outcomes

PO-1	Engage in critical thinking and pursue investigations/ research and development to solve practical problems.
PO-2	Communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO-3	Demonstrate higher level of professional skills to tackle multidisciplinary and complex problems related to VLSI System Design.
PO-4	Model and offer solutions to issues related to device, IC design, testing and EDA tool development
PO-5	Comprehend the state of the art VLSI technologies
PO-6	Characterize and design analog, digital, RF and mixed signal subsystems meeting given constraints under deep sub micron environment

CURRICULUM
M.Tech. VLSI System Design

1st Semester

S.No.	Code	Course Title	L-T-P	Credits
1	EC26001	Device Modeling	3-0-0	3
2	EC26003	Analog IC Design	3-0-0	3
3	EC26005	Digital IC Design	3-0-0	3
4	EC260XX	Professional Elective – I	3-0-0	3
5	EC260XX	Professional Elective – II	3-0-0	3
6	EC26007	Analog IC Design Lab	0-1-2	2
7	EC26009	Digital IC Design Lab	0-1-2	2
		Total Credits		**19**

2nd Semester

S.No.	Code	Course Title	L-T-P	Credits
1	EC26002	Physical Design Automation	3-0-0	3
2	EC26004	Mixed Signal Design	3-0-0	3
3	EC260XX	Professional Elective – III	3-0-0	3
4	EC260XX	Professional Elective – IV	3-0-0	3
5	EC260XX	Professional Elective – V	3-0-0	3
6	EC26006	Physical Design Automation/FPGA Design Lab	0-1-2	2
7	EC26008	Mixed Signal Design Lab	0-1-2	2
8	EC26096	Minor Project	0-0-0	2
		Total Credits		**21**

3rd Semester

S.No.	Code	Course Title	L-T-P	Credits
1	EC26089	Seminar and Technical Writing	0-0-0	2
2	EC26093	Comprehensive Viva-Voce	0-0-0	2
3	EC26097	Dissertation: Part-A	0-0-0	8
4	EC26091	Summer Internship/Research Experience	0-0-0	2
			Total Credits	**14**

4th Semester

S.No.	Code	Course Title	L-T-P	Credits
1	EC26098	Dissertation: Part-B	0-0-0	12
			Total Credits	**12**

Professional Elective Courses:

Professional Elective – I		
S.No.	**Code**	**Course Title**
1	EC26021	FPGA Design
2	EC26023	Nano-electronic Materials and Devices
3	EC26025	Quantum Computing
4	EC16027	IoT Architecture & Computing

Professional Elective – II		
S.No.	**Code**	**Course Title**
1	EC26027	Microchip Fabrication Techniques
2	EC26029	VLSI Test and Testability
3	EC26031	Advanced VLSI Interconnects
4	EC16031	Deep Learning Architectures

Professional Elective – III		
S.No.	**Code**	**Course Title**
1	EC26022	Low Power IC Design
2	EC26024	Power Management IC Design
3	EC16022	Hardware and Software Co-design of Embedded Systems
4	EC26026	Advanced Computer Architecture

Professional Elective – IV		
S.No.	**Code**	**Course Title**
1	EC26028	Electronic Packaging and 3D IC Technologies
2	EC26030	CMOS RFIC Design
3	EC26032	Embedded System and RTOS
4	EC26034	VLSI Design Verification

Professional Elective – V		
S.No.	**Code**	**Course Title**
1	EC26036	Hardware Description Languages
2	EC26038	Reliability of Devices and Circuits
3	EC26040	VLSI Architectures
4	EC26042	ASIC Design

The Overall Credit Structure

Course Category	**Credits**
Program Core	23
Professional Electives	15
Minor Project	2
Seminar and Technical Writing	2
Summer Internship/Research Experience	2
Comprehensive Viva-Voce	2
Dissertation	20
Total Graded Credit Requirement	66

SYLLABI

M.Tech. VLSI SYSTEM DESIGN

1st Semester

EC26001 **3-0-0 (3)**

Device Modeling

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand the governing equations along with their boundary conditions.
CO-2	Develop a sound physical and intuitive understanding of semiconductor devices
CO-3	Achieve ability to make key decisions while designing applications specific semiconductor devices.
CO-4	Simulate characteristics of a simple device using MATLAB, SPICE or other tools.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	3	2	2	1	1	3
CO-2	2	3	1	1	1	2
CO-3	2	3	2	2	1	1
CO-4	1	2	1	1	1	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction: significance of modeling

Review of crystal structure: Unit cell and Miller Indices, Doping, Band Structure, Effective Mass, Density of states, Electron Mobility, Semiconductor Statistics- Fermi- Dirac function and carrier concentration calculation.

Semiclassical Transport Theory: Distribution Function, Boltzmann Transport Equation (BTE), Relaxation-Time Approximation (RTA), Scattering and Mobility.

Drift-Diffusion (DD) model: Drift-Diffusion Model Derivation and dielectric relaxation time, Taylor series expansion and Finite Difference method, Normalization, Scaling and Linearization of Poisson's Equation and Scharfetter–Gummel Discretization of the Continuity Equation, Generation and Recombination models, Derivation of SRH model, Boundary conditions, Gummel's Iteration Method and Newton's Method, Drift-Diffusion Application example.

Hydrodynamic Modeling: As extension of DD model, Carrier Balance, Energy balance and momentum balance Equations, Direct solution scheme through Monte Carlo simulations

Quantum Transport models: Tunneling, Schrodinger equation and free particle, potential step, potential barrier, Transfer Matrix Approach, Quantum Mechanical corrections to standard approach.

Models for DD, Hydrodynamic simulations, Mobility and G-R models, Selected Examples: SPICE Diode and MOSFET Models and Their Parameters

Learning Resources:

Text Books:

1. C. Snowden, "Introduction to Semiconductor Device Modelling", World Scientific, 2011.

2. S. M. Sze and Kwok K. Ng, Physics of Semiconductor Devices, John Wiley & Sons, 2006, 3rd Edition.
3. Mark Lundstrom, Fundamentals of Nanotransistors, World Scientific, 2017.
4. Yannis Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, Oxford University Press, 2011, 2nd Edition.
5. Supriyo Datta, Lessons from Nanoelectronics: A New Perspective on Transport (In 2 Parts), World Scientific, 2018, 2nd Edition.

Reference Books:

1. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995, 1st Edition.
2. N. Arora, MOSFET Models for VLSI Circuit Simulation: Theory and Practice, Springer-Verlag Wein New York, 1993.
3. Norman G. Einspruch and Gennady Gildenblat, Advanced MOS Device Physics, Academic Press, 1989.
4. Y. Leblebici and S. M. Kang, Hot-Carrier Reliability of MOS VLSI Circuits, Springer Science + Business Media, LLC, 1993.
5. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/108/105/108105188/)

EC26003 **3-0-0 (3)**

Analog IC Design

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand the biasing styles and limitations
CO-2	Design CMOS analog basic building blocks
CO-3	Evaluate different CMOS amplifier topologies and design for given specifications
CO-4	Comprehend the stability issues of the systems and design two stage amplifier

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	1	1	_	–
CO-2	3	3	3	3	3	–
CO-3	3	3	2	3	2	–
CO-4	2	3	2	3	3	–

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Review of MOSFET device characteristics: Second order effects, MOS small signal Model, Capacitances, body bias effect, Current biasing, voltage biasing, Technology biasing, Relative comparision and limitations

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Mismatch inaccuracies, Design solutions to minimize mismatch inaccuracies.

Single stage amplifier: Analytical justification of operating region suitable for amplification/switching , Design of CS amplifier with different loads, Limitations of diode connected load, Improving output impedance of CS amplifier through feedback ,small signal analyses of common gate and common drain topologies and their frequency response with parasitic affects, significance of cascode, design of cascode amplifier and with ideal current source load and practical cascode load, Limitations of cascode, folded cascode amplifier and design with parasitics.

Differential amplifier: Significance of differential signaling, Limitations of quasi differential amplifier, Design of differential amplifier with current source load and diode connected load and small signal analyses, errors due to mismatch, replication principle, qualitative analysis, common mode response, gilbert cell, Common centroid layout.

Operational amplifier: characterization, two stage OP amp, small signal analysis, Miller compensation, effect of RHP zero on stability, Lead compensation, constant g_m biasing, design of biasing circuit independent of process and temperature variations.

Band Gap Reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, curvature correction, Design of BGR under low voltage conditions.

Learning Resources:

Text Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2nd Edition.
2. Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, 6th Edition.
3. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGrawHill, 1994.

Reference Books:

1. Randall L. Geiger, Phillip E. Allen and Noel R. Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 1989.
2. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2nd Edition.
3. Paul G. A. Jespers and Boris Murmann, Systematic Design of Analog CMOS Circuits, Cambridge University Press, 2017.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/117101105)

EC26005 **3-0-0 (3)**

Digital IC Design

Pre-Requisites: **None**

Course Outcomes:

CO-1	Design CMOS inverters with specified noise margin and propagation delay.
CO-2	Design an Inverter with different logic styles and analyse the performance
CO-3	Design building blocks of combinational and sequential circuits using CMOS logic
CO-4	Design Synchronous Systems meeting timing constraints.
CO-5	Study various architectures in the organization of volatile and non-volatile memories using 1-bit memory cells along with periphery circuits to improve access time and power consumption.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	2	3	2	-
CO-2	2	1	1	1	2	2
CO-3	2	1	1	2	3	1
CO-4	1	1	2	2	3	1
CO-5	1	1	1	2	3	-

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

MOS Inverters: Structure and Operation of MOS Transistor (MOSFET), MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effect, MOSFET Capacitances, CMOS Inverter- Static and switching characteristics, Delay-Time Definitions, Calculation of Delay Times, Inverter Design with Delay Constraints Estimation of Interconnect Parasitics, Power Consumption in CMOS Gates.

Designing Combinational & Sequential Logic Gates in CMOS: Static CMOS design- ratioed logic, pass transistor logic, transmission gate logic, Dynamic CMOS Design, Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles, Nonbistable Sequential Circuits, Logic Style for Pipelined Structures.

Timing Issues in Digital Circuits: Introduction, Synchronous Timing basics, Clock Skew and Jitter, Clock distribution techniques, Clock Generation and Synchronization.

Designing Arithmetic Building Blocks: Introduction, The Adder: Circuit and Logic Design, Multipliers: Shifters, Power Considerations in Datapath Structures.

Designing Memory: Introduction, Semiconductor Memories - An Introduction, The Memory Core: RAM, ROM, Memory Peripheral Circuitry.

Learning Resources:

Text Books:

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson, 2003, 2nd Edition.
2. John P. Uyemura, CMOS Logic Circuit Design, Springer, 2001.
3. John P. Uyemura, Introduction to VLSI Circuits and Systems, Wiley, 2002.

Reference Books:

1. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits, McGraw-Hill, 2003, 3rd Edition.
2. Charles Hawkins, Jaume Segura and Payman Zarkesh-Ha, CMOS Integrated Digital Electronics: A First Course, IET, 2012.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/108106158)

EC26007 **0-1-2 (2)**

Analog IC Design Lab

Pre-Requisites: **EC26003**

Course Outcomes:

CO-1	Understand the significance of different biasing styles and apply for analog circuits
CO-2	Design basic building blocks for analog CMOS circuits
CO-3	Comprehend the stability issues of the systems and design OP-amp fully compensated against process, supply and temperature variations
CO-4	Identify suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system.
CO-5	Design Analog integrated circuits with parasitic effects.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	3	1	1	1	1	–
CO-2	3	2	3	1	3	–
CO-3	3	3	3	3	3	–
CO-4	3	3	3	3	3	–
CO-5	3	3	3	3	3	–

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

All circuits till post layout

Lambda calculation for PMOS & NMOS, Transconductance plots, Single transistor amplifier with different loads, CS amplifier with source degeneration, Cascode amplifier.

Current sinks: Basic current sink, Cascode current sink.

Current sources: Basic current source, Cascode current source.

Current mirrors: Basic current mirror, Wilson current mirror, Cascode current mirror, Feedback topologies, CMOS differential amplifier with current mirror load.

Two stage Operational amplifier.

Learning Resources:

Text Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2nd Edition.
2. Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, 6th Edition.
3. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw Hill, 1994, 1st Edition.

Reference Books:

1. Randall L. Geiger, Phillip E. Allen and Noel R. Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 1989.
2. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2nd Edition.

EC26009 **0-1-2 (2)**

Digital IC Design Lab

Pre-Requisites: **EC26005**

Course Outcomes:

CO-1	Design of combinational and sequential building blocks using HDL
CO-2	Synthesize the building blocks of digital circuits and perform timing analysis targeting standard cell based semicustom design methodology.
CO-3	Implement a digital system using standard cell based semicustom design methodology.
CO-4	Analyse the performances of a digital system employing a few power optimization techniques.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	-	1	2	1
CO-2	2	1	-	2	1	1
CO-3	2	-	2	1	1	–
CO-4	2	-	-	2	3	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Cycle 1

Design and Simulation of CMOS Inverter to study the transfer Characteristics by varying the design constraints using EDA Tools

Design and Simulation of logic gates using various logic styles and compare the performance

Cycle 2

Design the following building blocks employing various architectures and develop HDL models:

32-bit Parallel adder using 8-bit adder module, 32-bit Shift register using 8-bit Shift register module,

Combinational and sequential multipliers: 8 x 8 multiplier, 16 X 16 multipliers

Perform the functional simulation, Static Timing Analysis and post synthesis timing verification

RTL to GDS-II: Design any System as a case Study

EDA Tools: Cadence Tools, Synopsys Tools

Learning Resources:

Text Books:

1. Samir Palnitkar, Verilog HDL, Pearson Education, 2003, 2nd Edition.
2. Erik Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Pearson, 2011.
3. Joseph Cavanagh, Verilog HDL: Digital Design and Modeling, CRC Press, 2007.

Reference Books:

1. Joseph Cavanagh, Verilog HDL Design Examples, CRC Press, 2018.
2. Blaine Readler, Verilog by Example: A Concise Introduction for FPGA Design, Full ARC Press, 2011.

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/108/106/108106158/)

2nd Semester

EC26002 **3-0-0 (3)**

Physical Design Automation

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
CO-2	Adapt the design algorithms to meet the critical design parameters.
CO-3	Learn various layout optimization techniques and map them to the algorithms.
CO-4	Develop proto-type EDA tool and test its efficacy.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	1	1	3
CO-2	2	1	2	1	2	2
CO-3	1	1	2	1	2	3
CO-4	1	2	3	2	2	3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multichip modules.

Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin-based methods, neighbor pointers, corner stitching, multi-layer operations.

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Learning Resources:

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, Kluwer Academic, 1999, 3rd Edition.
2. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2022, 2nd Edition.

3. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer, 2008.

Reference Books:

1. Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008, 1st Edition
2. Sabih H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2008, 2nd Edition.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2009.

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/106/105/106105161/)

EC26004 **3-0-0 (3)**

Mixed Signal Design

Pre-Requisites: **EC26003, EC26005**

Course Outcomes:

CO-1	Understand the necessity of mixed signal systems
CO-2	Analyze Op-Amp to meet the mixed signal specifications.
CO-3	Design CMOS comparators to meet the high-speed requirements of digital circuitry.
CO-4	Develop efficient data converter circuits for mixed signal systems

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	1	2	1	–
CO-2	2	1	3	2	1	1
CO-3	2	1	3	2	3	2
CO-4	3	1	3	3	2	3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Review of two stage OP amp: Parasitic effects on design of 2 stage OP amp, wide swing cascode current mirrors, design of rugged biasing circuit with temperature independent compensation, Challenges in mixed signal circuit design.

Switched Capacitor Circuits:

Constituents: Op-Amp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic Insensitive Integrators, Signal-Flow-Graph Analysis. Design of filters based on switched capacitor circuits,

Sample-and-Hold Circuits: Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, effect of offset and application of switched capacitor circuits to minimize offset errors, Parasitic affects.

Comparators: Ideal comparator, practical model of comparator, resolving capability, propagation delay, small signal analysis, conditions for slewing, evaluation of propagation delay for single pole and two pole comparators, Design of Linear response comparators, slew-rate limited comparators, comparators with positive feedback, analysis of latched Comparators, Architecture of High-speed comparators, self-biased comparators, push pull comparators.

Data Converters: Classification, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity Integrating Converters, Design of Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Principles of Sigma-Delta ADC, Testing of data converters.

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations of the Second-

Order Small-Signal Model, PLL characterization and Design Example. Jitter and Phase Noise, Period Jitter, P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators, LC Oscillators, phase Noise of Oscillators, jitter and Phase Noise in PLLS.

Learning Resources:

Text Books:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits" McGraw Hill Education, 2017, 2nd Edition.
3. R. Jacob Baker, CMOS: Mixed-Signal Circuit Design, Wiley, 2008, 2nd Edition.

Reference Books:

1. Roubik Gregorian and Gabor C. Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.
2. Roubik Gregorian, Introduction to CMOS Op-Amps and Comparators, Wiley, 2008.
3. Rui Paulo da Silva Martins and Pui-In Mak, "Analog and Mixed-Signal Circuits in Nanoscale CMOS", Springer, 2024.

Other Suggested Readings:

1. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc22_ee34/preview)

EC26006 **0-1-2 (2)**

Physical Design Automation / FPGA Design Lab

Pre-Requisites: **EC26002, EC26005**

Course Outcomes:

CO-1	Apply the constraints posed by the VLSI fabrication technology to design automation tools using graph algorithms
CO-2	Simulate partitioning algorithms viz., KL algorithm and simulated annealing algorithms.
CO-3	Optimize floor planning using time driven floor planning algorithm and hierarchical tree based methods
CO-4	Optimize routing using two terminal and multi terminal algorithms.
CO-5	Students get exposure to the resources of latest FPGA devices and FPGA Design Flow
CO-6	Applying various low power techniques and analyse the performance

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	2	2	1	3	–
CO-2	1	1	1	1	1	1
CO-3	2	2	2	2	2	3
CO-4	2	2	2	2	2	3
CO-5	2	3				2
CO-6	2			3	3	3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Cycle 1

- Graph algorithms
  - Graph search algorithms
    - Depth first search
    - Breadth first search
  - Spanning tree algorithm
    - Kruskal's algorithm
  - Shortest path algorithm
    - Dijkstra algorithm
    - Floyd-Warshall algorithm
  - Steiner tree algorithm
- Computational geometry algorithm
  - Line sweep method
  - Extended line sweep method

Cycle 2

- Partitioning algorithms

- Group migration algorithms
  - Kernighan –Lin algorithm
  - Extensions of Kernighan-Lin algorithm
    - Fiduccias –Mattheyses algorithm
    - Goldberg and Burstein algorithm
- Simulated annealing and evolution algorithms
  - Simulated annealing algorithm
  - Simulated evolution algorithm
- Metric allocation method

- Floor planning algorithms
  - Constraint based methods
  - Integer programming based methods
  - Rectangular dualization based methods
  - Hierarchical tree based methods
  - Simulated evolution algorithms
  - Time driven Floorplanning algorithms
- Routing algorithms
  - Two terminal algorithms
    - Maze routing algorithms
      - Lee's algorithm
      - Soukup's algorithm
      - Hadlock algorithm
    - Line-Probe algorithm
    - Shortest path based algorithm
  - Multi terminal algorithm
    - Stenier tree based algorithm
      - SMST algorithm
      - Z-RST algorithm

FPGA Lab

Cycle 1

Design, Simulate, Synthesize the following Combinational Ckts targeting 7 series FPGA

8-bit -bit low power high speed adder

High Speed and low power 16/32/64-bit adder using an 8-bit adder

16x16 bit multiplier using IP Core, CORDIC multiplier

Design, Simulate, Synthesize the following Sequential circuits targeting 7 series

FPGA a clock divider, FIFO using IP core

Cycle 2

Implement any System targeting Artix-7 series FPGA employing low power techniques while meeting target speed

Learning Resources:

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, Kluwer Academic, 1999, 3rd Edition.

2. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2022, 2nd Edition.
3. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer, 2008.
4. Frank Bruno, FPGA Programming for Beginners, Packt, 2021, 1st Edition
5. Frank Bruno and Guy Eschemann, The FPGA Programming Handbook, Packt, 2024, 2nd Edition.

Reference Books:

1. Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.
2. Sabih H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2008, 2nd Edition.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2009.

Other Suggested Readings:

1. NPTEL Courses (https://elearn.nptel.ac.in/shop/iit-workshops/completed/lab-workshop-fpga-architecture-and-programming-using-verilog-hdl/?v=c86ee0d9d7ed)

EC26008 **0-1-2 (2)**

Mixed Signal Design Lab

Pre-Requisites: **EC26004**

Course Outcomes:

CO-1	Implement discrete time signal processing circuits
CO-2	Implement layout techniques specific to mixed signal IC design
CO-3	Design OP-amp for mixed signal environment
CO-4	Design a high-speed comparator with high resolving capability
CO-5	Design data converters and RF circuits for mixed signal environment.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	3	1	1	1
CO-2	1	1	3	1	1	2
CO-3	2	1	2	2	2	3
CO-4	2	1	2	2	2	3
CO-5	2	2	3	2	3	3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation

2) comparator design a. linear Response b. Slew-rate limited

Cycle 2:

3) Switched capacitor circuits

i. Parasitic sensitive integrator

ii. Parasitic insensitive integrator

iii. Delay free integrators

iv. Low Pass filter

4) Data converters (ADC, DAC for given specifications)

5) Layouts and parasitic extraction

Learning Resources:

Text Books:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.

2. Roubik Gregorian and Gabor C. Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.

Reference Books:

1. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
2. Alan Hastings, The art of Analog Layout, Wiley, 2005.

Other Suggested Readings:

1. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc23_ee142/preview)

EC26096 **0-0-0 (2)**

Minor Project

Pre-Requisites: **None**

Course Outcomes:

CO-1	Apply engineering principles to real-world projects
CO-2	Plan and monitor project tasks individually or as a team
CO-3	Demonstrate practical experience in project execution
CO-4	Communicate project findings clearly through reports and presentations

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	3	3	3	3	3	
CO-2	2	2	2	2	2	
CO-3	2	2	2	2	2	
CO-4	1	1	1	1	1	

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Description:

Students are expected to choose real world or relevant problems and apply the engineering principles learned, to solve the problem through building prototypes or simulations or writing codes or establishing processes/synthesis/correlations etc. The department constituted panel can decide the suitability and worthiness of the project

Evaluation Criteria:

The student will be evaluated by the panel based on the below criteria. Weightage for each criterion will be determined by the panel and will be informed to the students.

Criteria	Description	Weightages
I	Identification of Problem Domain	
II	Study of Existing Systems and establishing clear objectives	
III	Planning of project and work distribution within the team	
IV	Proper Documentation and Technical Writing	
V	Presentation and Response to questions	

Evaluation Criteria-CO Mapping

CO / Criteria	CO1	CO2	CO3	CO4
I	X			
II	X			
III		X	X	
IV				X
V				X

3rd Semester

EC26089 **0-0-0 (2)**

Seminar and Technical Writing

Pre-Requisites: **None**

Course Outcomes:

CO-1	Consolidate ideas based on expert talks attended
CO-2	Prepare a well-organized report employing elements of critical thinking and technical writing
CO-3	Demonstrate the ability to describe, interpret and analyze the subject matter and develop competence in presenting

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2		2			3
CO-2	2		2			3
CO-3	2		2			3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Description:

In Seminar and Technical Writing, every student is expected to prepare a well-organized report based on one / all of the following:

- by attending at least 5 expert lectures/ invited talks/ Seminar/ Popular lectures etc. organized by the institute/any of the departments, ideally in a specific domain or with the same theme.
- prepare a business or marketing plan based on patent search

The student is expected to consolidate the ideas from these lectures/patent searches and may even include material from other sources to strengthen the content of the report. The student should prepare a well-organized report based on the above and present it to the panel constituted by the department, for evaluation.

Evaluation Criteria:

The student will be evaluated by the panel based on the below criteria.

Criteria	Description	Weightages
I	Clarity on the topic	
II	List of lectures attended	
III	Report	
IV	Presentation	
V	Response to questions	

Evaluation Criteria-CO Mapping

CO / Criteria	CO1	CO2	CO3
I	X		
II	X		
III		X	
IV			X
V			X

EC26093 **0-0-0 (2)**

Comprehensive Viva-Voce

Pre-Requisites: **None**

Course Outcomes:

CO-1	Comprehend the knowledge gained in the course work
CO-2	Demonstrate the ability in problem solving
CO-3	Communicate effectively using engineering terminology

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	3	3	3	3		
CO-2	3	3	3	3		
CO-3	2	2	2	2		

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Description:

In Comprehensive viva-voce each student will be evaluated for their overall comprehension of the course work and laboratory training that they have undergone. The students will be expected to answer questions orally, write down simple equations, draw plots, schematics, write simple code etc. as questioned by the panel. Assessment will be done by the panel based on the student response.

EC26097 **0-0-0 (8)**

Dissertation: Part-A

Pre-Requisites: **None**

Course Outcomes:

CO-1	Identify a topic in advanced areas of VLSI System Design.
CO-2	Review literature to identify gaps and define objectives and scope of the work.
CO-3	Employ the ideas from literature and develop research methodology.
CO-4	Develop a model, experimental set-up and / or computational techniques necessary to meet the objectives.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	3	2	3	1		3
CO-2	3	2	3	1		3
CO-3	3	3	3	3	3	3
CO-4	3	3	3	3	3	3

1 - Slightly; 2 - Moderately; 3 - Substantially

Description:

Students are expected to choose real-world contemporary problem and apply the engineering principles learned, to solve the problem through building prototypes or simulations or writing codes or establishing processes/synthesis/correlations etc. The department constituted panel will decide the suitability and worthiness of the project

Dissertation Evaluation:

i. The dissertation shall be submitted as per the schedule given in the academic calendar.
ii. The dissertation supervisor will periodically review the progress of the student and finally give his/her assessment of the work done by the student.
iii. The Dissertation Part – A will be evaluated for 100 marks, with the following weightages:

Sub-component	**Weightage**
a) Periodic evaluation by Guide	40 marks
b) Mid-term review	20 marks
c) End Semester viva-voce examination	40 marks

Evaluation Criteria

The student will be evaluated by the panel based on the below criteria. Weightage for each criterion will be determined by the panel and will be informed to the students.

Criteria	Description	Weightages
I	Selection of Topic	
II	Literature Survey	
III	Defining the Objectives and Solution Methodology	
IV	Performance of the Task	

Evaluation Criteria - CO Mapping:

CO / Criteria	CO1	CO2	CO3	CO4
I	X			
II		X		
III			X	
IV				X

Refer to the M.Tech. – Regulations for any further information regarding mid-term review and end semester evaluation, etc.

EC26091 **0-0-0 (2)**

Summer Internship/Research Experience

Pre-Requisites: **None**

Course Outcomes:

CO-1	Apply engineering principles to real-world problems, gaining practical experience
CO-2	Plan, manage and execute the work with ethical consideration
CO-3	Review the social and environmental impact of the work
CO-4	Communicate the learnings through report and presentation

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	3	3	3	3	3	
CO-2	2	2	2	2	2	
CO-3						3
CO-4						

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Description:

Every student has to undergo either a Summer Internship / Research project. The summer internship may be undergone in an Industry/Research organization or any premier academic Institution, including NIT Warangal for 6-8 weeks. The research project shall be registered under the guidance of any faculty member in the institute. The student is required to submit a report and present the work before an evaluation committee, nominated by the Head of the Department.

Evaluation Criteria:

The student will be evaluated by the panel based on the below criteria. Weightage for each criterion will be determined by the panel and will be informed to the students.

Criteria	Description	Weightages
I	Relevance of the area of work	
II	Performance of the Task	
III	Crucial learnings from the work	
IV	Report Preparation	
V	Presentation and Response to questions	

Evaluation Criteria-CO Mapping

CO / Criteria	CO1	CO2	CO3	CO4
I	X			
II		X		
III			X	
IV				X
V				X

4th Semester

EC26098 **0-0-0 (12)**

Dissertation: Part-B

Pre-Requisites: **EC26097**

Course Outcomes:

CO-1	Identify the materials and methods for carrying out experiments/develop a code.
CO-2	Execute the research methodology with a concern for society, environment and ethics
CO-3	Analyse, discuss and justify the results/trends and draw valid conclusions.
CO-4	Prepare the report as per recommended format and present the work orally adhering to stipulated time.
CO-5	Explore the possibility to publish/present a paper in peer reviewed journals/conference proceedings without plagiarism.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2		3	3	2	3
CO-2	2		3	3	2	3
CO-3	3		3	3	2	3
CO-4	3	3	3	3	3	3
CO-5	3	3	3			3

1 - Slightly; 2 - Moderately; 3 - Substantially

Description:

Students are expected to choose real-world contemporary problem and apply the engineering principles learned, to solve the problem through building prototypes or simulations or writing codes or establishing processes/synthesis/correlations etc. The department constituted panel will decide the suitability and worthiness of the project.

Dissertation Evaluation:

i. The dissertation shall be submitted as per the schedule given in the academic calendar.
ii. The dissertation supervisor will periodically review the progress of the student and finally give his/her assessment of the work done by the student.
iii. The Dissertation Part – B will be evaluated for 100 marks, with the following weightages:

Sub-component	**Weightage**
a) Periodic evaluation by Guide	40 marks
b) Mid-term review	20 marks
c) End Semester viva-voce examination	40 marks

Evaluation Criteria:

The student will be evaluated by the panel based on the below criteria as a continuation of Dissertation Part A. Weightage for each criterion will be determined by the panel and will be informed to the students.

Task	Description	Weightages
IV	Performance of the Task	
V	Dissertation Preparation	
VI	Review (Presentation & Understanding)	
VII	Viva-Voce	
VIII	Publications /Possibility of publication	

Evaluation Criteria-CO Mapping:

CO / Criteria	CO1	CO2	CO3	CO4	CO5
IV	X	X			
V				X	
VI			X		
VII				X	
VIII					X

Refer to the M.Tech. – Regulations for any further information regarding mid-term review and end semester evaluation, etc.

Professional Electives

Professional Elective – I

EC26021 **3-0-0 (3)**

FPGA Design

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand FPGA design flow.
CO-2	Identify the building blocks of commercially available FPGA/CPLDs.
CO-3	Develop VHDL/Verilog models and synthesize targeting for Vertex, Spartan FPGAs.
CO-4	Develop parameterized library cells and implement system designs using parameterized cells.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	2	2	1	1	–
CO-2	2	1	2	3	3	–
CO-3	2	1	2	3	2	1
CO-4	3	–	1	2	2	–

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction to FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA.

Design Examples using PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter.

FPGAs/CPLDs: Programming Technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGA/CPLD.

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures. FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA

CASE STUDY – Applications using Kintex-7, Viretex-7, Artix-7.

Learning Resources:

Text Books:

1. John V. Oldfield and Richard C. Dorf, Field Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems, Wiley-Interscience, 1995, 1st Edition.
2. Frank Bruno, FPGA Programming for Beginners, Packt, 2021.
3. Frank Bruno and Guy Eschemann, The FPGA Programming Handbook, Packt, 2024, 2nd Edition.
4. Stephen D. Brown, Robert J. Francis, Jonathan Rose and Zvonko G. Vranesic, Field Programmable Gate Arrays, Springer Science+Business Media, LLC, 1992, 1st Edition.

Reference Books:

1. Clive Maxfield, The Design Warrior's Guide to FPGAs: Devices, Tools and Flows, Elsevier-Newnes, 2004.
2. Data sheets of Artix-7, Kintex-7, Virtex-7.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/117108040)

EC26023 **3-0-0 (3)**

Nano-electronic Materials and Devices

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand the physics and materials for Nanoelectronics
CO-2	Understand the scaling issues
CO-3	Explain the need for non-classical and non-silicon based devices
CO-4	Analyse the performance of novel devices

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	1	1	1	1
CO-2	2	1	1	2	1	1
CO-3	2	1	2	2	2	1
CO-4	2	1	3	2	2	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Overview: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore's Law and Koomey's law.

Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO2 vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability - Qbd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, Metal gate transistor : Motivation, requirements, Integration Issues.

Non-classical MOS transistor: Requirements, and Novel devices

SOI - PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues.

Vertical transistors - FinFET and Cylindrical gate FET.

Novel devices: Tunnel FET, Negative-Capacitance (NC) FET.

Metal source/drain junctions - Properties of Schottky junctions on Silicon, Germanium and

compound semiconductors -Workfunction pinning.

Emerging Nano MOSFETs: strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors MOSFETs in the context of channel quantization and strain, Hetero structure MOSFETs, exploiting novel materials, strain, quantization. CNT, Graphene, Nanotubes, nanorods and other nano-structures.

Learning Resources:

Text Books:

1. Y. Taur and T. Ning, “Fundamentals of Modern VLSI devices” Cambridge University Press, 2022, 3rd Edition.
2. Nicollian and J. R. Brews “MOS (Metal Oxide Semiconductor) Physics and Technology” Wiley, 2002, 1st Edition
3. Brundle, C. Richard, Evans, Charles A. Jr., Wilson, Shaun “Encyclopedia of Materials Characterization”, Butterworth-Heinemann Manning Publications Co., 1992,

Reference Books:

1. Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017. 2nd Edtiton.
2. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009
3. Related research papers.

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/117/108/117108047/)

EC26025 **3-0-0 (3)**

Quantum Computing

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand the principles of quantum computation qubit
CO-2	Analyze multi-qubit systems and protocols
CO-3	Apply quantum measurement and entanglement concepts
CO-4	Design and implement quantum algorithms and circuits

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	1	2	1	1
CO-2	2	1	3	2	2	2
CO-3	2	1	3	2	2	2
CO-4	2	1	3	2	2	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Review of Quantum Mechanics and Motivation for Quantum Computation Qubit: The qubit state - matrix and Bloch sphere representation - computational basis unitary evolution.

Multi-qubit states - No-cloning theorem - Superdense coding - Pure states to Bell states – Bell inequalities. Protocols with multi-qubits: Swapping - Teleportation - gates: CNOT - Toffoli gate - NAND - FANOUT - Walsh Hadamard.

Measurement: Projective operators - General, Projective and POVM measure, Ensemble: Density operators - pure and mixed ensemble - time evolution – post measurement density operator. Composite systems: Partial trace - Reduced density operator - Schmidt decomposition, Purification bipartite entanglement.

Quantum computing: Classical computing using qubits - Quantum parallelism - Deutsch's algorithm - Deutsch Josza algorithm.

Quantum circuits: Basic gates - ABC decomposition - Gray codes - Universal gates - Principle of deferred and implicit measurements - Quantum Fourier transform - applications: phase estimation, order finding - factoring, discrete logarithm and hidden subgroup problems - Role of prime factoring in classical cryptography - search algorithms. Quantum error correcting codes, Physical realization of qubits.

Learning Resources:

Text Books:

1. M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010, 10th Anniversary Edition
2. Chris Bernhardt, Quantum Computing for Everyone, The MIT Press, 2019.
3. Ray LaPierre, Introduction to Quantum Computing, Springer, 2021.

Reference Books:

1. Quantum Theory: Concepts and Methods, Asher Peres, Kluwer Academic Publishers, 1993.
2. Venkateswaran Kasirajan, Fundamentals of Quantum Computing: Theory and Practice, Springer, 2021.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/106106232)

EC16027 **3-0-0 (3)**

IoT Architecture & Computing

Pre-Requisites: **None**

Course Outcomes: At the end of the course, the student will be able to:

CO1	Understand the various concepts of the IoT and their technologies.
CO2	Develop the IoT application using different hardware platforms
CO3	Understanding and Implement the various IoT Protocols
CO4	Understand the basic principles of cloud computing.
CO5	Develop and deploy the IoT application into cloud environment

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	2	2	2	1
CO-2	2	1	2	2	2	1
CO-3	1	1	1	2	2	1
CO-4	1	1	1	1	1	1
CO-5	1	1	1	1	2	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction to IoT – definition, Characteristics, Complete Architectural Stack, IoT enabling Technologies and Challenges. **Sensors and Hardware for IoT** – Hardware Platforms – Arduino, Raspberry Pi, Node MCU. A Case study with any one of the boards and data acquisition from sensors.

IoT Protocols – Infrastructure protocol (IPV4/V6/RPL), Identification (URIs), Transport (Wifi, Lifi, BLE), Discovery, Data Protocols, Device Management Protocols. – A Case Study with MQTT/CoAP usage-IoT privacy, security and vulnerability solutions.

Cloud Architecture Basics – Fundamentals of cloud, cloud architecture standards and interoperability-Cloud types; IaaS, PaaS, SaaS. Benefits and challenges of cloud computing, public, private clouds community cloud, Development environments for service development; Amazon, Azure, Google App cloud platform in industry

IoT and the Cloud - Role of Cloud Computing in IoT, AWS Components, Connecting a web application to AWS, IoT using MQTT, AWS IoT Examples. Security Concerns, Risk Issues, and Legal Aspects of Cloud Computing- Cloud Data Security

Case studies with architectural analysis: IoT applications, Smart City, Smart Water, Smart Agriculture, Smart Energy, Smart Healthcare, Smart Transportation, Smart waste management.

Learning Resources:

Text books:

1. Pethuru Raj and Anupama C. Raman by The Internet of Things: Enabling Technologies, Platforms, and Use Cases, CRC Press.

2. Adrian McEwen, Designing the Internet of Things, Wiley, 2013, 1st Edition

3. Singh, Rajesh. Gupta, LoviRaj. Gehlot, Anita. Singh, Bhupendra. Swain, Mahendra, “Internet of Things with Raspberry Pi and Arduino” United Kingdom: Taylor & Francis Limited, 2021.

Professional Elective – II

EC26027 **3-0-0 (3)**

Microchip Fabrication Techniques

Pre-Requisites: **None**

Course Outcomes:

CO-1	Explain the unit fabrication process steps
CO-2	Analyze process yield and yield measurement for a process
CO-3	Propose the process flow for MOS devices
CO-4	Construct the circuit stick diagrams and circuit layout using the design rules

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	3	2	1	1
CO-2	2	2	2	3	3	1
CO-3	3	2	3	3	3	2
CO-4	1	1	3	2	1	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Overview of semiconductor industry, unit process steps for fabrication

Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Contamination sources, Clean room construction; Oxidation: dry oxidation, wet oxidation; Photolithography: Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect.

Etching: Dry etching, Wet etching, resist stripping; Doping: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2; Deposition: CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapor phase epitaxy, molecular beam epitaxy; Chemical mechanical polishing; Metallization.

Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices.

Design rules, stick diagrams and layout.

Packaging: Chip characteristics, package functions, package operations

Yield Measurement: Types of Yields, Models, Effect of Contamination on Yield

Learning Resources:

Text Books:

1. Peter Van Zant, Microchip Fabrication, McGraw Hill, 2014, 6th Edition.
2. S.M. Sze, VLSI Technology, McGraw-Hill, 2017, 2nd Edition (Indian).
3. Sorab K Gandhi, VLSI Fabrication Principles: Silicon and Germanium Arsenide, Wiley, 1994, 2nd Edition.

Reference Books:

1. James D Plummer, Peter B Griffin and Michael D Deal, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson, 2009, 1st Edition.
2. Stephen A Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2001, 2nd Edition.
3. C.Y. Chang and S.M. Sze, ULSI Technology, McGraw Hill, 2000, 2nd Edition

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/108/108/108108113/)

EC26029 **3-0-0 (3)**

VLSI Test and Testability

Pre-Requisites: **None**

Course Outcomes:

CO-1	Identify the significance of testable design
CO-2	Understand the concept of yield and identify the parameters influencing the same.
CO-3	Specify fabrication defects, errors and faults
CO-4	Implement combinational and sequential circuit test generation algorithms
CO-5	Identify techniques to improve fault coverage

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	2	2	2	1	1
CO-2	1	3	1	2	2	1
CO-3	2	2	1	2	2	1
CO-4	1	1	1	1	2	2
CO-5	1	1	1	2	2	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.

Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.

Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain-based testing method.

D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan-based design.

Classical scan-based design, System level DFT approaches Test pattern generation for BIST, Circular BIST. BIST Architectures. Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Learning Resources:

Text Books:

1. M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000.

Reference Books:

1. Stroud, “A Designer’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002
2. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/117/105/117105137/)

EC26031 **3-0-0 (3)**

Advanced VLSI Interconnects

Pre-Requisites: **None**

Course Outcomes:

CO-1	Get an insight on transmission line parameters of VLSI interconnects
CO-2	Understand the novel solutions on future VLSI Interconnects
CO-3	Analyze the inductive effects in interconnects
CO-4	Analyze the effect of quantum effects in interconnects

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	1	1	-
CO-2	2	1	2	3	2	1
CO-3	3	2	3	2	3	3
CO-4	3	2	3	2	3	3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction: Introduction to VLSI Interconnects, the distributed RC interconnect model, Elmore delay in interconnects, Scaling effects in interconnects, simulation and delay mitigation in RC interconnects.

Inductive Effects: Inductive effects in interconnects, Distributed RLC interconnect model, Transmission line equations, When to consider the inductive effects? Equivalent Elmore model for RLC interconnects, Two-pole model of RLC interconnects from ABCD parameters, RLC interconnect simulation.

Skin effect and Electromigration: Origin of the skin effect, Effective resistance at high frequencies, Power dissipation due to interconnects, Electromigration in interconnects, Mitigation of electromigration.

Crosstalk: Capacitive coupling in interconnects, Cross-talk effects in two identical interconnects, mitigation techniques, Analysis and simulation of coupled interconnects. Extraction of capacitance, Extraction of inductance, Estimation of interconnect parameters from S-parameters.

Quantum Effects: Quantum conductance, quantum capacitance, kinetic inductance, Graphene nanoribbon interconnects, Analysis and simulation of Interconnect considering quantum effects.

Learning Resources:

Text Books:

1. Ashok K. Goel, High-Speed VLSI Interconnects, 2007.
2. Y.S. Diamand, Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications, 2009.

Reference Books:

1. H.S Philip Wong and Deji Akinwande, Carbon nanotube and Graphene Device Physics, 2011.
2. Related research papers.

Other Suggested Readings:

1. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc22_ee125/preview)

EC16031 **3-0-0 (3)**

Deep Learning Architectures

Pre-Requisites: **None**

Course Outcomes:

CO1	Understand the basic concepts of neural networks and deep learning methods
CO2	Know the basic model types used in deep learning, e.g., Convolutional Neural Networks (CNNs), Recurrent Neural Networks (RNNs), and Generative Adversarial Networks (GANs)
CO3	Build and train deep neural networks and identify key architecture parameters
CO4	Modify state-of-the-art deep learning architectures for a new dataset/task. And re-train and tune hyper parameters of several classes of deep learning methods.
CO5	Know the suitability of specific deep learning methods to various real world data domains such as the ones arising from text, images, and videos.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	1	1	2	1
CO-2	2	2	1	1	2	1
CO-3	2	2	1	3	3	1
CO-4	2	2	1	2	2	1
CO-5	2	1	1	2	2	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction to Deep Learning: Neural Networks, The basic building blocks of deep learning, Training of Neural Networks.

Convolutional Neural Networks (CNNs): CNN architectural details, CNN architectures – LeNet, AlexNet, VGG, Resenet, Googlenet, Inceptionnet. Training a CNNs: weights initialization, batch normalization, hyperparameter optimization, Understanding and visualizing CNNs.

Recurrent Neural Networks (RNNs): RNNs, Need of RNN, The basic building blocks of RNNs and other architectural details, Study of some special RNN architectures: GRU, LSTM, Seq2Seq models, Attention mechanism.

Unsupervised deep learning: Self-organized maps, Autoencoders

Generative models: Architectural and training of Generative Adversarial Networks (GANs), Restrictive Boltzmann Machines (RBMs), Stacking RBMs, Belief nets, Learning sigmoid belief nets, Deep belief nets Adversarial attacks on Neural Networks.

Learning Resources:

Text Books:

1. Ian Good fellow, Yoshua Bengio and Aaron Courville, Deep learning, In preparation for MIT Press, Available online: http://www.deeplearningbook.org, 2016

Reference Books:

1. Satish Kumar, Neural Networks - A Class Room Approach, Second Edition, Tata McGraw-Hill, 2013.
2. Charu C. Aggarwal Neural Networks and Deep Learning Springer International Publishing, 2018
3. Andrew W. Trask, Grokking Deep Learning Manning Publications

Professional Elective – III

EC26022 **3-0-0 (3)**

Low Power IC Design

Pre-Requisites: **None**

Course Outcomes:

CO-1	Identify clearly the sources of power consumption in a given VLSI Circuit.
CO-2	Analyze and estimate dynamic and leakage power components in a DSM VLSI Circuit.
CO-3	Choose the types of SRAMs/ DRAMs for the given Low power applications.
CO-4	Design low power arithmetic circuits and systems.
CO-5	Decide at which level of abstraction is advantageous to implement low power techniques in a VLSI system design.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	1	1	1
CO-2	1	1	1	1	2	1
CO-3	1	2	2	2	3	2
CO-4	2	2	2	3	2	3
CO-5	2	1	3	1	2	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Low Power CMOS VLSI design: Introduction: Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation.

Circuit Techniques for Low Power Design: Design for Low Power, Multiple Vth techniques, Dynamic Vth techniques.

Standard Adder Cells, Review of CMOS Adders Architectures and performance Comparison, Low Voltage Low Power Design Techniques, Current Mode Adders.

Review of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison.

Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques.

Architectural Techniques for Low Power: Parameters effecting power dissipation, Variable frequency, Dynamic voltage Scaling, Dynamic Voltage and Frequency Scaling, Reduced VDD, Architectural clock gating, Power gating, Multi-voltage, Optimizing memory power.

Low Power Implementation Techniques: Library Selection, Clock Gating, Timing Impact due to Clock gating, Gate-level power optimization techniques, Power Optimization for Sleep Mode.

Learning Resources:

Text Books:

1. Kiat Seng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Tata McGraw Hill, 2009.
2. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002.

Reference Books:

1. Abdellatif Bellaouar, Mohamed Elmasry, Low-Power Digital VLSI Design: Circuits and Systems, Springer, 2012.
2. Jan Rabaey, Low Power Design Essentials, Springer, 2009.

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/106/105/106105034//)

EC26024 **3-0-0 (3)**

Power Management IC Design

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand why power management circuits are needed in a VLSI system
CO-2	Understand different components of a power management system with focus on dc-dc converters
CO-3	Design a chip level dc-dc converter from a given system level specifications
CO-4	Apply top-down design approach of a dc-dc converter topology

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	3	2	3	1	1	1
CO-2	2	2	3	1	1	1
CO-3	3	2	3	2	2	2
CO-4	2	2	3	2	2	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction to Power Management and Voltage Regulation: Introduction to Power Management and Voltage Regulators Need of power management, power management applications, classification of power management, power delivery of a VLSI system, power conversion, discrete vs. integrated power management, types of voltage regulators (switching Vs linear regulators) and applications, converter's performance parameters (voltage accuracy, power conversion efficiency, load regulation, line regulation, line and load transient response, settling time, voltage tracking), local Vs remote feedback, kelvin sensing, Point-of-Load (POL) regulators.

Principles of Linear Voltage Regulators: Linear Regulators Low Drop-Out Regulator (LDO), Source and sink regulators, shunt regulator, pass transistor, error amplifier, small signal and stability analysis, compensation techniques, current limiting, power supply rejection ratio (PSRR), NMOS vs. PMOS regulator, current regulator.

Switching DC-DC Converters: Design and Control Technique: Switching DC-DC Converters and Control Techniques Types (Buck, boost, buck-boost), power FETs, choosing L and C, PWM modulation, leading, trailing and dual edge modulation, Losses in switching converters, output ripple, voltage Vs current mode control, CCM and DCM modes, small signal model of dc-dc converter, loop gain analysis of un-compensated dc-dc converter, type-I, type-II and type-III compensation, compensation of a voltage mode dc-dc converter, compensation of a current mode dc-dc converter, hysteretic control, switched capacitor dc-dc converters.

Systematic Design of DC-DC Converters: Top-down Design Approach of a DC-DC Converter Selecting topology, selecting switching frequency and external components, sizing power FETs, segmented power FET, designing gate driver, PWM modulator, error amplifier, oscillator, ramp generator, feedback resistors, current sensing, PFM/PSM mode for light load, effect of parasitic on reliability and performance, current limit and short circuit protection, soft start control, chip level layout and placement guidelines, board level layout guidelines, EMI considerations.

Emerging Technologies in Power Management: Introduction to Advanced Topics in Power Management

Digitally controlled dc-dc converters, digitally controlled LDOs, adaptive compensation, dynamic voltage scaling (DVS), Single-Inductor Multiple-Outputs (SIMO) Converters, dc-dc converters for LED lighting, Li-ion battery charging circuits.

Learning Resources:

Text Books:

1. Switch-Mode Power Supplies: SPICE Simulations and Practical Designs, Christophe P Basso, BPB Publications, 2010.
2. Power Management Techniques for Integrated Circuit Design By Ke-Horng Chen, Wiley-Blackwell, 2016.

Reference Books:

1. Fundamentals of Power Electronics, 2nd edition by Robert W. Erickson, Dragan Maksimovic, Springer (India) Pvt. Ltd, 2005.
2. Bernhard Wicht, Design of Power Management Integrated Circuits, Wiley, 2024.

Other Suggested Readings:

1. NPTEL Courses (https://archive.nptel.ac.in/courses/108/106/108106159/)

EC1622 **3-0-0 (3)**

Hardware and Software Co-design of Embedded Systems

Pre-Requisites: **None**

Course Outcomes: At the end of the course, the student will be able to:

CO-1	Understand Hardware/Software Co-design
CO-2	Model the data flow and implement the same through software and hardware.
CO-3	Design the hardware controllers through Control Flow Graph Structures.
CO-4	Understand the design principles in SoC Architecture
CO-5	Design CORDIC and Crypto coprocessor architectures

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	--	1	--
CO-2	1	2	2	--	1	1
CO-3	1	2	2	--	1	1
CO-4	1	1	2	--	--	1
CO-5	--	--	--	--	--	--

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design.

Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph, Construction of the Data Flow Graph.

Architectures for Embedded Systems: a. Single processor – coprocessor architecture, mixed-signal architectures, multiprocessor architectures, reconfigurable architectures, Systems on Chip.

Performance Modeling: a. System-level performance modeling vs. low-level performance modeling. b. Modeling of system latency, energy consumption etc for hardware and software. c. Estimation of memory requirements.

System-Level Synthesis and Trade-off Analysis: a. Design of customized digital blocks. b. Hardware/software partitioning. Task binding. c. IP core integration and communication synthesis: Hardware and software interface synthesis. d. Hardware IP core synthesis: High-level synthesis: behavioral specification of hardware, module set allocation, resource binding, operation scheduling, controller design

Learning Resources:

Text Books:

1. Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010.
2. A. Doboli, E. Currie, “Introduction to Mixed-Signal Embedded Design”, Springer, 2010.
3. G. De Micheli, R. Ernst, W. Wolf, “Readings in Hardware/Software Co-Design”, Morgan Kaufman, 2002.
4. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998.

EC26026 **3-0-0 (3)**

Advanced Computer Architecture

Pre-Requisites: **None**

Course Outcomes: At the end of the course, the student will be able to:

CO-1	Understand the micro-architectural design of processors.
CO-2	Evaluate performance of different architectures with respect to various parameters
CO-3	Analyze performance of different ILP techniques
CO-4	Identify cache and memory related issues in multi-processors
CO-5	Understand the concept of NOC

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	--	2	2	1	1
CO-2	2	1	2	2	1	1
CO-3	1	1	2	3	1	1
CO-4	1	--	2	2	1	1
CO-5	--	--	1	--	--	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction to high performance computing, RISC philosophy and overview of pipelined architecture. Performance evaluation of pipelined architecture. Limitations of scalar pipelines, Instruction level parallelism.

Superscalar architecture: Instruction flow optimization, Handling branches, Advanced optimization in instruction flow, register flow techniques: Register renaming and out of order execution.

Advanced data flow techniques: Instruction reuse and value prediction, Memory data flow, advanced memory data flow architectures, performance evaluation of superscalar architectures.

Multi-threading, Simultaneous multithreaded (SMT) architectures, SMT architecture: Choices,

SMT performance on various designs, SMT architecture: OS impact and adaptive architectures

Multi scalar architecture, Multi-core Architectures, Multi-core Interconnect–NOC, Network on-Chip, Cache Coherence, Cache Consistency model, Dynamic Core architectures, GPGPU Architecture, CPU-GPU Integration.

Learning Resources:

Text Books:

1. J.L. Hennessy, and D.A. Patterson, Computer Architecture: A quantitative approach, 5th Edition, Morgan Kaufmann Publication, 2012.

2. J.P. Shen and M.H. Lipasti, Modern Processor Design, MCGraw Hill, Crowfordsville, 2005.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/106103182/)

Professional Elective – IV

EC26028 **3-0-0 (3)**

Electronic Packaging and 3D IC Technologies

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand the role of packaging in the computer, telecommunication, automotive, medical and consumer electronics industry
CO-2	Learn the fundamentals of electrical packaging design, design for reliability, thermal management
CO-3	Analyze the performance of various TSVs for 3-D ICs
CO-4	Identify the packaging materials with their appropriate properties

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	-	1	-
CO-2	1	1	1	-	1	-
CO-3	3	2	3	3	3	3
CO-4	2	1	2	2	3	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Functions of an Electronic Package, Packaging Hierarchy, Driving Forces on Packaging Technology. Materials for Microelectronic packaging, Packaging materials properties, ceramics, polymers and metals in packaging. Electrical Anatomy of systems packaging, signal distribution, power distribution, electromagnetic interference.

Through Silicon Via: Materials, properties of TSVs, fabrication of TSVs, challenges for TSV implementation. Modeling and performance analysis of Copper-based, CNT-based, GNR-based TSVs. Liners in TSVs.

3-D technology and Packaging Techniques: Silicon interposer technology, Through Silicon Vias (TSVs). Hybrid packaging technique, Silicon-Less Interconnect technology. 3D Integrated Architectures

Physical Design and Thermal Management Techniques for 3-D ICs

Case study: clock distribution networks for 3-D ICs, Trends in Packaging.

Learning Resources:

Text Books:

1. Vasilis F Pavlidis, E G Friedman, Three-Dimensional Integrated Circuit Design, Morgan Kaufmann Publishers, Elsevier, 2009.
2. Rao R. Tummala , Fundamentals of Microsystem Packaging, McGraw Hill, 2001.

Reference Books:

1. John H. Lau, Through-Slicon Vias for 3D Integration, McGraw Hill, 2012.
2. Related research papers.

Other Suggested Readings:

1. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc23_cs07/preview)

EC26030 **3-0-0 (3)**

CMOS RFIC Design

Pre-Requisites: **None**

Course Outcomes:

CO-1	Understand the design bottlenecks specific to RF IC design
CO-2	Identify noise sources and develop noise models for the devices and systems.
CO-3	Identify various Transmitter and receiver architectures
CO-4	Design various RF amplifiers

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	1	3	1	1	-
CO-2	2	1	2	3	1	2
CO-3	3	2	3	3	2	2
CO-4	3	3	2	3	3	3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Basic concepts of RF IC design: Design Bottle necks of RF IC design Non-linearity and Time invariance Sensitivity and dynamic range, Passive impedance transformation, RF radio receiver front end non-idealities and design parameters: Effects of nonlinearity, 1 dB compression point, Derivation of required noise figure at receiver front end, Required IIP_3 at receiver front end, Partitioning of required NF at receiver front end and IIP_3 into individual NF and IIP_3.

Noise: Noise sources in MOSFETs, Modeling of thermal noise and flicker noise, noise analog integrated circuits.

Transceiver architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests.

Low Noise Amplifier: Introduction, General Philosophy, Matching Networks, Comparison of Narrowband and wideband LNA.

Wideband LNA Design: DC Bias, Gain ad Frequency Response, Noise Figure.

Narrowband LNA: Principles, core amplifier design, noise figure, power dissipation, trade-offs between noise figure and power dissipation, noise contribution from other sources.

Mixers: Active mixer, modeling mixers, unbalanced mixer circuits, single balanced mixer circuit, double balanced mixer circuits, Quantitative description of Gilbert mixer, conversion gain, Distortion, analysis of Gilbert mixer. Passive mixers: switching mixer, distortion in unbalanced switching mixer, conversion gain and noise.

Frequency synthesizer: PLL based frequency synthesizer: Concepts of PLL, phase detector, charge pump, RF Synthesizer architectures, Frequency Dividers, VCO, LC oscillators, Ring oscillator, Phase noise, Loop filter and system design.

Learning Resources:

Text Books:

1. Bosco Leung, VLSI for wireless communication, Springer, 2011, 2nd Edition.
2. Behad Razavi, RF Microelectronics, Prentice Hall, 2011, 2nd Edition.

Reference Books:

1. Rovert Caverly, CMOS RFIC Design Principles, Artech House, 1st Edition, 2007
2. Hooman Darabi, Radio Frequency Integrated Circuits and Systems, Cambridge University Press, 2020, 2nd Edition.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/106103182/)

EC26032 **3-0-0 (3)**

Embedded Systems and RTOS

Pre-Requisites: **None**

Course Outcomes:

CO-1	Identify the functioning of embedded systems for different applications.
CO-2	Develop embedded system programming skills.
CO-3	Design, implement and test an embedded system.
CO-4	Identify the unique characteristics of real-time embedded systems.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	-	1	-
CO-2	2	1	2	1	1	-
CO-3	2	3	2	2	3	2
CO-4	2	1	1	-	2	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction to Embedded Computing: Embedded systems Overview, Characteristics ofembedded computing applications, Design Challenges, Common Design Metrics, Processor Technology, IC Technology, Trade-offs.

Process of Embedded System Development: The development process, Requirements, Specification, Architecture Design, Designing Hardware and Software components, system Integration and Testing.

Hardware platforms: Types of Hardware Platforms, Single board computers, PC Add-oncards, custom-built hardware platforms, ARM Processor, CPU performance, CPU power consumption, Bus-based computer systems, Memory devices, I/O devices, component interfacing, Designing with microprocessors, system level performance analysis.

Program Design and Analysis: components for Embedded programs, Models of programs, Assembly, Linking, and loading, basic compilation techniques, software performance optimization, program level energy and Power analysis, Program validation and Testing.

Real-Time Operating Systems: Architecture of the kernel, Tasks and Task Scheduler, Scheduling algorithms, Interrupt Service Routines, Semaphores, Mutex, Mailboxes, Message queues, Event Registers, Pipes, Signals, Timers, Memory management, Priority Inversion problem. Overview of off-the shelf operating systems-MicroC/OS II, Vxworks, RT Linux.

Overview of Hardware –Software co design

Learning Resources:

Text Books:

1. Wayne Wolf: Computers as Components-Principles of Embedded Computer System Design, Morgan Kaufmann Publisher-2006, 2nd Edition

2. David E-Simon: An Embedded software Primer, Pearson Education, 2007, 1st Edition
3. K.V.K.K. Prasad Real-Time Systems: Concepts Design and Programming, Dreamtech Press, 2005.

EC26034 **3-0-0 (3)**

VLSI Design Verification

Pre-Requisites: **None**

Course Outcomes: At the end of the course, the student will be able to:

CO-1	Apply scheduling and allocation algorithms for VLSI verification
CO-2	Develop logic optimization for sequential circuits
CO-3	Construct binary decision diagram and apply temporal logic
CO-4	Implement simulation-based verification

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	2	1	1
CO-2	2	1	2	3	2	2
CO-3	2	1	2	3	2	2
CO-4	2	1	2	2	1	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction: Introduction to Digital VLSI Design Flow, High Level Design Representation, Transformations for High Level Synthesis.

Scheduling and Allocation: Scheduling, Allocation and Binding Problem, Scheduling Algorithms, Binding and Allocation Algorithms, Allocation Techniques: Clique Partitioning, Left- Edge Algorithm, Iterative Refinement.

Logic Optimization and Synthesis: Two level Boolean Logic Synthesis, Heuristic Minimization of Two-Level, Finite State Machine Synthesis, Multilevel Implementation.

Binary Decision Diagram: Introduction and construction, Ordered Binary Decision Diagram, Operations on Ordered Binary Decision Diagram, Ordered Binary Decision Diagram for Sequential Circuits.

Temporal Logic: Introduction and Basic Operations on Temporal Logic, Syntax and Semantics of CLT, Equivalence between CTL Formulas

Model Checking: Verification Techniques, Model Checking Algorithm, Symbolic Model Checking

Learning Resources:

Text Books:

1. G. De Micheli. Synthesis and optimization of digital circuits, 1994, 1st Edition
2. Douglas L Perry Harry D Foster, Applied Formal Verification, McGraw Hill, 2005, 1st Edtion
3. William K Lam, Hardware Design Verification: Simulation and Formal Method-based Approaches, Prentice Hall, 2008.

Reference Books:

1. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2004, 2nd Edition,
2. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1992, 1st Edition
3. M. L. Bushnell and V. D. Agrawal, “Essentials of Electronic Testing” ,3rd Kluwer Academic Publishers 2002
4. IEEE Standard for Universal Verification Methodology Language Reference Manual," in *IEEE Std 1800.2-2017*, vol., no., pp.1-472, 26 May 2017

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/106103016).

Professional Elective – V

EC26036 **3-0-0 (3)**

Hardware Description Languages

Pre-Requisites: **None**

Course Outcomes: At the end of the course, the student will be able to:

CO-1	Differentiate sequential language and concurrent language.
CO-2	Design combinational logic circuits using VHDL.
CO-3	Design sequential logic circuits using VHDL.
CO-4	Model Analog circuits using Verilog AMS.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	2	2	1	2	-
CO-2	1	1	1	1	3	3
CO-3	1	1	1	1	2	3
CO-4	2	2	2	1	1	3

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Verilog: About Verilog, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading.

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential Code to Design Combinational Circuits.

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to OneHot.

System Verilog: Verilog +, Coverage, Randomization, Assertion, functional coverage, Object oriented programming, define – parameter.

Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling.

Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior.

Learning Resources:

Text Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2003, 2nd Edition
2. Chris Spear, System Verilog for Verification: A Guide to Learning the Testbench Language Features, Springer, 2012, 3rd Edition
3. Kenneth S. Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004.

Reference Books:

1. Joseph Cavanagh, Verilog HDL Design Examples, CRC Press, 2018, 1st Edition
2. Blaine Readler, Verilog by Example: A Concise Introduction for FPGA Design, Full ARC Press, 2011.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/106105165).

EC26038 **3-0-0 (3)**

Reliability of Devices and Circuits

Pre-Requisites: **None**

Course Outcomes:

CO-1	Define the reliability of electronic device and circuit
CO-2	Understand the failure mechanisms of electronic device and circuit
CO-3	Understand the concept of yield in electronic manufacturing
CO-4	Resolve the reliability issues in VLSI design
CO-5	Predict the circuit performance using reliability models

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	1	1	2	-	1
CO-2	2	1	1	2	1	2
CO-3	2	1	2	1	-	1
CO-4	2	3	2	3	2	3
CO-5	3	3	2	2	2	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Background and Introduction: Definitions of reliability, failure modes, mechanisms, Basic concepts – Reliability functions, Relationship between these functions – Baths tubs curve – Exponential failure density and distribution functions - Expected value and standard deviation of Exponential distribution – Measures of reliability – MTTF, MTTR, MTBF

Introduction to mathematical methods for reliability: Failure rates, Normal distribution function, Six Sigma, Exponential, Weibull and Lognormal distributions for reliability modeling. Manufacturing yields.

Physics of failure-based models for: Mass transport-induced failures (electromigration and stress voiding), Electronic charge-induced failures (Dielectric breakdown, Hot carrier effects, Electrical over-stress and Electrostatic discharge), Environmental damage (moisture ingress, corrosion, radiation damage), Degradation of interconnects (solder creep and fatigue).

Circuit Performance considering NBTI, PBTI, oxide breakdown, random telegraph noise, radiation damage, impact of parasitic effects, process temperature variation, Electromagnetic compatibility (EMC), Electromagnetic Interference (EMI) and Electrostatic Discharge (ESD).

Introduction to semiconductor device packaging: Materials and processes used for semiconductor device packaging, stresses induced because of packaging.

Learning Resources:

Text Books:

1. M. Ohring, Reliability and Failure of Electronic Materials and Devices, First Edition, Academic Press, 1998, 2nd Edition
2. J.W. McPherson, Reliability Physics and Engineering, Second Edition, Springer, 2013, 2nd Edition

3. Yuan Taur and T. Ning, “Fundamentals of Modern VLSI Devices,” Cambridge University Press, 1998.
4. J.Ross, Microelectronic Failure Analysis, Sixth Edition, ASTM International, 2011.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/112105267).

EC26040 **3-0-0 (3)**

VLSI Architectures

Pre-Requisites: **None**

Course Outcomes:

CO-1	Design of RISC architecture and controller for a specific instruction set.
CO-2	Improve the performance of RISC processor by employing pipelining.
CO-3	Translate DSP algorithm into an efficient architecture and study the design of different building blocks of DSP architectures.
CO-4	Estimate the effect of folding, unfolding and retiming techniques on the performance of DSP architectures.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	2	2	1	1	2	1
CO-2	2	2	1	3	3	1
CO-3	2	1	2	2	2	2
CO-4	3	1	2	2	2	2

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Overview of the features of Instruction set architectures of CISC, RISC and DSP processors.

CPU performance and its factors, evaluating the performance.

Design of RISC processor**:** Building datapath and Control, multicycle implementation.

Enhancing the performance with pipelining**:** An overview of pipelining, pipelined datapath, Pipelined Control unit, various hazards of pipelining, Hazard free pipelined RISC implementation.

Multiprocessors: Introduction, Multiprocessors connected by a single bus, Multiprocessors connected by a network, Network Topologies, Evolution versus revolution in Computer Architecture.

Representation of DSP Algorithms, data flow graph representations, loop bound and iterative bound, algorithms for computing iteration bound.

Pipe lining and parallel processing: Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

Different techniques to improve the performance VLSI Architectures: Retiming, Unfolding and Folding techniques.

Learning Resources:

Text Books:

1. D.A, Patterson And J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, Elsevier, 2011, 4th Edition
2. Keshab Parhi, VLSI digital signal processing systems design and implementations, Wiley 1999

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/108105157)

EC26042 **3-0-0 (3)**

ASIC Design

Pre-Requisites: **None**

Course Outcomes:

CO-1	Design of ASIC library.
CO-2	Develop programmable ASIC logic cells.
CO-3	Design I/O cells and interconnects.
CO-4	Identification of new developments in SOC and low power design.

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6
CO-1	1	2	2	1	2	1
CO-2	1	2	3	2	1	1
CO-3	2	3	2	3	2	2
CO-4	2	2	2	3	1	1

1 - Slightly; **2 - Moderately;** **3 - Substantially**

Syllabus:

Introduction: Types of ASIC's, Design Flow, CMOS Logic.

Traditional Design Flow: Specification and RTL Coding, Dynamic Simulation, Constraints, Synthesis and Scan Insertion, Formal Verification, Static Timing Analysis, Placement, Routing and Verification, Engineering Change Order, Physical Compiler Flow Physical Synthesis

Example Design: Initial Setup, Traditional Flow, Pre-Layout Steps, Post-Layout Steps

Physical Compiler Flow

Technology Library: Technology Libraries, Logic Library Basics, Delay calculation

Partitioning and Coding Styles: Partitioning for Synthesis, General guidelines, Logic Inference

Constraining Designs: Environment and Constraints, Advanced Constraints, Clocking issues

OPTIMIZING DESIGNS: Design Space Exploration, Total Negative Slack, Compilation Strategies, Optimization techniques

Design for Test: Types of DFT, Scan Insertion

Programmable ASIC Design: CLB, IOB, Programmable Interconnect of Xilinx Devices

Learning Resources:

Text Books:

1. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, Kluwer Academic, 2002, 2nd Edition
2. Michel John Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley Professional, 2008.

Reference Books:

1. Vaibbhav Taraate, ASIC Design and Synthesis: RTL Design using Verilog, Springer Nature Singapore, 2021, 1st Editon
2. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys® Design CompilerTM and PrimeTime®, Springer, 2012.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/117103125).