NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL



Honors in

VLSI System Design

(for students of B.Tech., ECE)

(w.e.f. 2021-22)

Department of

Electronics and Communication Engineering

SCHEME OF INSTRUCTION

Honors Program – VLSI System Design

S.No	Course Code	Course Title	L	T	P	Credits	Sem
1	EC5204	Analog IC Design	3	0	0	3	V
2	EC5216	VLSI Architectures	3	0	0	3	V
3	EC5252	Mixed Signal Design	3	0	0	3	VI
4	EC5265	Hardware-Software Co-design	3	0	0	3	VI
5	EC5201	Microchip Fabrication Techniques	3	0	0	3	VII
6	EC5267	VLSI Design Verification	3	0	0	3	VIII
		Total				18	

Course Code: EC5204	Analog IC Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand the significance of different biasing styles and apply them aptly for different circuits
CO2	Design all basic building blocks like sources, sinks, mirrors, up to layout level.
CO3	Comprehend the stability issues of the systems and should be able to design OpAmp fully Compensated against process, supply and temperature variations.
CO4	Identify the suitable different topologies of the constituent sub systems and corresponding circuits as per the specifications of the system.
CO5	Design Analog integrated system completely upto tape-out including parasitic effects.

Detailed Syllabus:

MOS FET device I/V characteristics, second order effects, Capacitances, body bias effect, Biasing Styles, MOS small signal Model, NMOS verses PMOS devices.

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references.

Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stage with source degeneration, source follower, CG stage, Gain boosting techniques, Cascode, folded cascode, choice of device models.

Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, replication principle, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion, gilbert cell

Operational amplifier-characterization, 2 stage OP amp, process and temperature independent compensation, output stage.

Band Gap Reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, constant g_m biasing, speed and noise issues, case study, curvature correction.

PTAT, CTAT, Bandgap circuit, start-up circuit, curvature correction Design. Negative feedback amplifier design with Nyquist criteria analysis.

Learning Resources:

Text Books:

1. Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.
4. Design of Analog CMOS Integrated Circuit, Behad Razavi McGraw Hill Education, 2nd Edition 2017

Course Code: EC5216	VLSI Architectures	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO	Design of RISC architecture and controller for a specific instruction set.
CO	Improve the performance of RISC processor by employing pipelining.
CO	Translate DSP algorithm into an efficient architecture and study the design of
CO 4	Estimate the effect of folding, unfolding and retiming techniques on the performance of DSP architectures.

Detailed Syllabus:

Introduction: Overview of the features of Instruction set architectures of CISC, RISC and DSP processors, CPU performance and its factors, evaluating the performance.

Design of RISC processor: Building datapath and Control, multicycle implementation.

Enhancing the performance with pipelining: An overview of pipelining, pipelined datapath, Pipelined Control unit, various hazards of pipelining, Hazard free pipelined RISC implementation

Multiprocessors: Introduction, Multiprocessors connected by a single bus, Multiprocessors connected by a network, Network Topologies, Evolution versus revolution in Computer Architecture, Representation of DSP Algorithms, data flow graph representations, loop bound and iterative bound, algorithms for computing iteration bound

Pipe lining and parallel processing: Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power, Different techniques to improve the performance VLSI Architectures: Retiming, Unfolding and Folding techniques

Learning Resources:

Text Books:

1. D.A, Patterson And J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier, 2011.
2. Keshab Parhi, VLSI digital signal processing systems design and implementations, Wiley 1999

Course Code: EC5252	Mixed Signal Design	Credits 3-0-0: 3

Prerequisites: Analog and Digital IC Design

Course Outcomes: At the end of the course, the student will be able to:

CO1	Understand the necessity of mixed signal systems and demonstrate corresponding layout
CO2	Design basic cells like OpAmp to meet the mixed signal specifications.
CO3	Design comparators to meet the high speed requirements of digital circuitry.
CO4	Design a complete mixed signal system that includes efficient data conversion and RF

Detailed Syllabus:

Review: Simple CMOS Current Mirror, Common-Source Amplifier, Source-Follower, Source-Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain Stage, Process and temperature independent compensation, Ahuza's compensation, nested miller compensation, dynamic offset cancellation techniques.

Basic Building Blocks, OpAmp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator , Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit.

Performance of Sample-and-Hold Circuits, Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Bipolar and BiCMOS Sample-and-Holds, Translinear Gain Cell, Translinear Multiplier

Comparator Specifications Input Offset and Noise, Hysteresis, Using an OpAmp for a Comparator, Input-Offset Voltage Errors, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, speed of Multi-Stage Comparators, Latched Comparators, Latch-Mode Time Constant, Latch Offset, Examples of CMOS and BiCMOS Comparators, Input-Transistor Charge Trapping, Examples of Bipolar Comparators,

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity

Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate for Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters.

Multi-Bit Successive-Approximation**,** Algorithmic (or Cyclic) A/D Converter, Ratio-Independent Algorithmic Converter, Pipelined A/D Converters, One-Bit-Per-Stage Pipelined Converter,1.5 Bit Per Stage Pipelined Converter, Pipelined Converter Circuits,

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL characterization and Design Example. Jitter and Phase Noise, Period Jitter, P-Cycle Jitter, Adjacent Period Jitter,

other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators, LC Oscillators, phase Noise of Oscillators, jitter and Phase Noise in PLLS

Learning Resources:

Text Books:

1. Design of CMOS Phase-Locked Loops From Circuit level to Architecture Level, Behzad Razavi, Cambridge University Press, 2020.
2. Understanding Delta-Sigma Data Converters, Richard Schreier, Shanthi Pavan and Gabor C Temes, Wiley, 2nd Edition, 2017.
3. David A Johns, Ken Martin: Analog IC design, Wiley 2008.
4. R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986
5. Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008

Course Code: EC5265	Hardware / Software Co-Design	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Understand Serial and parallel communication protocols.
CO2	Model data flow and implement the same through software and hardware.
CO3	Operate data flow using USB and CAN bus for PIC microcontrollers.
CO4	Design embedded Ethernet for Rabbit processors.
CO5	Design CORDIC and Crypto coprocessor.

Detailed Syllabus:

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design.

Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.

Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph4.4 Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph.

Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor.

System on Chip: The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor.

Learning Resources:

Text Books:

1. Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010.

2. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998.

Course Code: EC5201	Microchip Fabrication Techniques	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Explain the unit fabrication process steps
CO2	Explain the functions of packaging
CO3	Analyze process yield and yield measurement for a process
CO4	Propose the process flow for novel MOS devices
CO5	Construct the circuit layout using the design rules

Detailed Syllabus:

Overview of semiconductor industry, unit process steps for fabrication, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement; Contamination sources, Clean room construction;

Oxidation: dry oxidation, wet oxidation;

Photolithography: Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect.

Etching: Dry etching, Wet etching, resist stripping; Doping: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2; Deposition: CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy; Chemical mechanical polishing; Metallization.

Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices.

Design rules, stick diagrams and layout.

Packaging: Chip characteristics, package functions, package operations

Learning Resources:

Text Books:

1. Microchip fabrication, Peter Van Zant McGraw Hill, 1997.
2. Silicon VLSI Technology: Fundamentals, Practice and Modeling , Plummer, J.D., Deal, M.D. and Griffin, P.B., Prentice-Hall , 2000, 3rd Ed.
3. ULSI technology , C.Y. Chang and S.M. Sze, McGraw Hill, 2000.
4. VLSI Fabrication principles, S.K. Gandhi, John Wiley and Sons, NY, 1994.
5. VLSI technology, S.M. Sze, McGraw-Hill Book company, NY, 1988.

Course Code: EC5267	VLSI Design Verification	Credits 3-0-0: 3

Course Outcomes:

At the end of the course, the student will be able to:

CO1	Specify the formal verification techniques.
CO2	Implement formal test plan process.
CO3	Implement simulation based verification.
CO4	Model hardware interfaces with concurrency constructs.
CO5	Apply IEEE 1850 property specification language and IEEE1800 Verilog assertions.

Detailed Syllabus:

Verification process: Verification plan, Debug Cycle, Simulation and Output data, Testbench development.

Current verification techniques: HDL Software simulator, Accelerated simulation, Process-Based Accelerator techniques, Hardware emulation, FPGA prototyping.

Introduction to formal techniques and property specification: Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process.

Techniques for proving properties: Abstraction reduction, Compositional reasoning, Counter abstraction, Gradual Exhaustive formal verification.

Final system simulation: Module verification, Full simulation from a simulation, Full Simulation from a formal verification.

IEEE 1850 PSL Property specifications and IEEE 1800 Verilog assertions: Introduction, Operations and keywords, PSL Boolean and temporal layer, Introduction to IEEE 1800 System Verilog, Sequence and property, BNF 185 and BNF 223.

Introduction to Verification Methodology: Open verification Methodology (OVM), Universal verification methodology (UVM)

Learning Resources:

Text Books:

1. Douglas L Perry Harry D Foster, Applied Formal Verification, McGraw Hill, 2005.
2. William K Lam, Hardware Design Verification: Simulation and Formal Method-based Approaches, Prentice Hall, 2008.
3. IEEE Standard for Universal Verification Methodology Language Reference Manual," in *IEEE Std 1800.2-2017* , vol., no., pp.1-472, 26 May 2017