NATIONAL WORKSHOP ON

Clock and Data Recovery Circuits

18th December -22nd December, 2019)

Sponsored by:
Scheme for Promotion of Academic and Research Collaboration (SPARC), MHRD, GOI

Organized by:
Department of Electronics and Communication Engineering, NIT Warangal, India

Collaboration with:
University of Illinois at Urbanachampaign

Preamble:

Scheme for Promotion of Academic and Research Collaboration (SPARC) is a Ministry of Human Resource Development (MHRD), GOI initiative to improve research ecosystem in India. It supports national premier educational institutions by facilitating academic and research collaborations between Indian institutions and the best and selected institutions across the world's 28 nations. The collaborative educational networks will work on common issue of national or international relevance. It encourages international faculty, Indian institution visits and long-term stays to teach courses and conduct workshops for the benefit of Indian researchers and students in the selected research area. Also, it funds Indian students to visit and access the premier laboratories worldwide for training and experimentation. As an outcome patents, monographs, and world-class publications will be produced.

About NIT Warangal and Department:

NIT Warangal, formerly known as Regional Engineering College was established in 1959. Over the years it has developed into a premier institute of higher learning and is ranked among the top technical education institutions in India. There are 14 Departments offering eight undergraduate and 32 post-graduate programmes besides doctoral programmes. About 5000 students across the country and about 500 international students study on the campus. The Department of Electronics and Communication Engineering is one of the country's larger **ECE** departments among all NITs in India and one of the largest departments of the National Institute of Technology, Warangal (NITW). The ECE Department at NITW has been an international reputation of excellence in teaching, research and service. With excellent laboratory facilities and dedicated faculty, the department of ECE offers broad range of programs that include undergraduate(B.Tech) and post graduate (M.Tech) in Electronics Instrumentation, VLSI System design, Communication Systems and research (Ph.D) programs. The Department has strong Industry interaction and is involved in various Research & Consultancy projects in coordination with industry, Governments of India, Telangana & Andhra Pradesh.

Overview of the Course: Phase-locked loops (PLLs) are de-facto clock generators in digital, analog, and communication systems. They are used to: (i) generate clocks across a wide range of frequencies (MHz to GHz), (ii) clean-up noisy clocks, (iii) perform clock recovery, and (iv) provide frequency/phase modulation. In all these applications, they take up valuable resources in terms of area and power. PLLs have been conventionally implemented using analog architectures such as the charge-pump topology. Because they consume large area and are sensitive to transistor imperfections, more recently they are being realized using mostly digital architectures. However, both analog and digital PLLs suffer from fundamental noise, power, and bandwidth tradeoffs that must be carefully managed. This course seeks to provide the know-how to make these tradeoffs judiciously.

This course entails analysis and design of phase-locked loop (PLL) architectures and circuits. Emphasis will be on fundamental understanding, design intuition, and implementation of PLLs in modern-day CMOS processes. Topics include charge-pump phase-locked loops, noise properties

of PLLs, integer/fractional-N PLLs, digital PLLs, delay-locked loops, and injection-locked clock multipliers. Supply noise mitigation techniques will be covered in detailclock and data recovery circuits.

Workshop Objectives

The primary objectives of the course are as follows:

- Understanding of basic and advanced PLL architectures
- Modelling of PLLs
- Exposure to circuit design of building blocks
- Provide design intuitionClock and data recovery (CDR) architectures
- Identification and mitigation of the impact of supply noise
- Exposure to practical problems of PLL's CDRs and their solutions, through case studies

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Course Level: Postgraduate, Ph.D. scholars and Faculty of Engineering and final year UG students

Resource Persons:

Prof. Pavankumar Hanumolu,
Electrical and Computer Engineering
Coordinated Science Lab
University of Illinois at Urbana Champaign
USA

Dr Sreehari Rao Patri
Associate Professor
ECE Department
NIT Warangal Telangana

Dr P Muralidhar
Associate professor
ECE Department
NIT Warangal

Registration Fee Particulars: FREE of cost

Accommodation: All the selected participants will be provided in the institute visitors/hostel block on twin sharing @ **Rs.500/-** per participant per day. AC accommodation will be provided as per request according to institute norms (Rs 2000/- per day that can be shared by 3 people) subjected to the availability. No TA will be paid for the participants.

Eligibility: The programme is open to the Faculty and Ph.D scholars/PG students of Electronics and Communication Engineering and allied disciplines. Industry personnel working in the concerned/allied discipline can also attend.

How to apply: A filled application form in the prescribed format duly signed and sponsored by appropriate authorities (along with payment details) **should send scanned application form & proof for Fee paid details through e-mail to patri@nitw.ac.in.** After paying the fee participants are requested to fill the Google doc for confirmation of your interest to attend this workshop.
Also, the original hard copies of the application form & proof for Fee paid details must be submitted at registration desk on first day of reporting. The selection status will be intimated only through mail.

Selection Criteria: Selection will be done based on first-cum-first-serve basis and the confirmed candidates will be notified immediately. The maximum number of participants will **be 50 (Fifty)**. Additionally 10 participants from industry are allowed to participate. The list of selected participants will be notified in the institute web site www.nitw.ac.in and also, will be sent to their personal e-mail address.

Important Dates:

Last date for Application with fee: 10th December 2019
Confirmed Selection List by Email: 12th December 2019

Google Doc Link:
https://drive.google.com/open?id=1yQHb3pOorEJyRDokTZS4wAn3FgemuG6ZpBMyS94v1K0

A test will be conducted at the end of the course.
Candidates will be issued satisfactory certificates on successful completion of the course.

Coordinators:

Dr. Sreeharirao Patri, Associate Professor,
ECE Dept. NITW
Dr P MuralAidhar, Associate professor
ECE Dept. NITW
For any enquiries please contact:
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Mobile: 8332969357 / 9441342324/ 8332969359

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REGISTRATION FORM

1. Name :
2. Designation :
3. Institution :
4. E-mail :
5. Phone No. :
6. Payment Details : NA
   a) Transaction No. :
   b) Bank :
   c) Date :
   d) Amount :
7. Address :

8. Qualification :
9. Accommodation : Required /Not Required

Declaration

The information provided is true to the best of my knowledge. If selected, I agree to abide by the rules and regulations of the course and shall attend the course for the entire duration. I also undertake the responsibility to inform the coordinator in case, I am unable to attend the course.

Signature of the Participant

SPONSORSHIP CERTIFICATE

Dr. /Mr. /Ms. …….... is an employee/student of our Institute/Organization and is hereby sponsored to participate in the **FIVE day National SPARC-Workshop** on **"Clock and Data Recovery Circuits"**, sponsored by Scheme for Promotion of Academic and Research Collaboration **(SPARC), MHRD, GOI** during 18th to 22nd December 2019 at NIT Warangal.

Signature of Head of Department/Institution
(with seal)

Address for correspondence:

Dr. Sreehari Rao Patri
Associate Professor
Dept. of Electronics and Communication Engineering,
National Institute of Technology Warangal,
WARANGAL - 506 004, Telangana State, India.

Note: ***E-mail the scanned copies of filled-in and duly signed application form along with proof for Fee Payment Details & date to*** ***patri@nitw.ac.in***

Also, the original hard copies of the application form & proof for Fee paid details must be submitted at registration desk on first day of reporting

For any enquiries please contact:
Mobile: 8332969365 / 9705024365